

**REMARKS**

Claim 51 is amended. Claims 51-58 are pending in the application.

Applicant acknowledges the Examiner's indicated allowability of the subject matter of claim 58.

Claims 51-57 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Tseng, U.S. Patent No. 5,830,802. The Examiner is reminded by direction to MPEP§ 2131 that anticipation requires each and every element of a claim to be disclosed in a single prior art reference. Claims 51-57 are allowable over Tseng for at least the reason that Tseng fails to disclose each and every element in any of those claims.

As amended, independent claim 51 recites forming a polycrystalline thin film transistor layer over a transistor gate, forming a fluorine containing layer proximate the polycrystalline thin film transistor layer, and transferring fluorine into the polycrystalline thin film transistor layer, the transferred fluorine passivating the polycrystalline thin film transistor layer in the bottom-gated thin film transistor. The amendment to claim 51 is supported by the specification at, for example, page 8, lines 1-5 and lines 15-19; and page 13, lines 1-22. Tseng discloses formation of a dielectric layer 58 over a refractory silicide layer 56 and out-diffusing halogen from the silicide layer into overlying dielectric layer 58 which is subsequently removed to prevent halogen diffusion into underlying gate layers (Fig. 2 and col. 3, lines 11-20, 30-32 and 56-60). Tseng does not disclose the claim 51 recited transferring fluorine into a polycrystalline thin film transistor layer to passivate the polycrystalline thin film transistor layer in a bottom-gated thin film transistor. Accordingly, independent claim 51 is not anticipated by Tseng and is allowable over this reference.

Dependent claims 52-54 are allowable over Tseng for at least the reason that they depend from allowable base claim 51.

Independent claim 55 recites forming a polycrystalline thin film transistor layer over a transistor gate, forming a fluorine containing layer over the polycrystalline thin film transistor layer, and providing a buffering layer intermediate the thin film transistor layer and the fluorine-containing layer. The Examiner indicates at page 3 of the present action that Tseng discloses providing a buffering layer intermediate a thin film transistor layer and a fluorine-containing layer. The Examiner is mistaken. The Examiner relies on column 3, lines 15-25 to support the contention that Tseng teaches a buffering layer. Referring to this site of the Tseng disclosure, applicant notes that the layer being discussed is dielectric layer 58 which is deposited over a refractory metal silicide layer 56 as shown in Fig. 2. Fluorine is then diffused from metal silicide layer 56 into dielectric layer 58 as indicated at column 3, lines 30-33. Tseng does not disclose the claim 55 recited buffering layer intermediate a thin film transistor layer and a fluorine containing layer. Additionally, Tseng does not disclose the claim 55 recited transferring fluorine into a polycrystalline thin film layer from an overlying fluorine containing layer. Accordingly, independent claim 55 is not anticipated by Tseng and is allowable over this reference.

Dependent claims 56-58 are allowable over Tseng for at least the reason that they depend from allowable base claim 55.

For the reasons discussed above pending claims 51-58 are allowable. Accordingly, applicant respectfully requests formal allowance of such pending claims in the Examiner's next action.

Respectfully submitted,

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